CLAIMS

We claim:

1. A trench-gated MIS device formed in a semiconductor chip and comprising:

an active area containing transistor cells;

a gate metal area containing no transistor cells; and

a gate metal layer,

wherein a trench is formed in a pattern on a surface of the semiconductor chip, the trench extending from the active area into the gate metal area, the trench having walls lined with a layer of an insulating material, a conductive gate material being disposed in the trench, a top surface of the conductive gate material being at a level below a top surface of the semiconductor chip, a nonconductive layer overlying the active and gate metal areas, an aperture being formed in the nonconductive layer over a portion of the trench in the gate metal area, the aperture being filled with a gate metal such that the gate metal contacts the gate material in an area of contact within the trench.

2. The trench-gated MIS device of Claim 1 comprising a gate metal layer overlying the nonconductive layer in the gate metal area, the gate metal layer being in electrical contact with the gate material.

3. The trench-gated MIS device of Claim 2 wherein the gate metal layer extends longitudinally in a direction perpendicular to a direction of the trench in the gate metal area.

4. The trench-gated MIS device of Claim 1 wherein a width of the trench at the area of contact between the gate contact material and the gate material is greater than a width of the trench in the active area.

5. The trench-gated MIS device of Claim 1 wherein a first gate finger extends from the active area to the gate metal area, the area of contact between the

gate contact material and the conductive gate material being located in a second gate finger , the second gate finger being perpendicular to the first gate finger.

6. The trench-gated MIS device of Claim 5 wherein a width of the second gate finger is greater than a width of the first gate finger.

7. The trench-gated MIS device of Claim 5 wherein a width of the second gate finger is greater than a width of the trenches in the active area.

8. The trench-gated MIS device of Claim 5 wherein a width of the second gate finger is the same as a width of the first gate finger at an intersection between the first and second gate fingers.

9. The trench-gated MIS device of Claim 8 wherein the area of contact between the gate metal and the gate material does not extend into the intersection between the first and second gate fingers.

10. The trench-gated MIS device of Claim 9 wherein a width of the second gate finger is greater than a width of the first gate finger in the area of contact between the gate metal and the gate material.

11. The trench-gated MIS device of Claim 5 wherein the first gate finger ends at the second gate finger so as to form a T intersection.

12. The trench-gated MIS device of Claim 11 wherein a width of the second gate finger is greater than a width of the first gate finger.

13. The trench-gated MIS device of Claim 12 wherein a third gate finger extends from the active area, the third gate finger ending at the second gate finger so as to form a second T intersection.

14. The trench-gated MIS device of Claim 13 wherein the first and third gate fingers are located on opposite sides of the second gate finger.

15. The trench-gated MIS device of Claim 1 comprising first and second gate fingers extending from the active area to the gate metal area.

16. The trench-gated MIS device of Claim 15 wherein the first gate finger contains a first widened portion and second trench gate finger contains a second widened portion.

17. The trench-gated MIS device of Claim 16 wherein the aperture in the nonconductive layer overlies the first widened portion.

18. The trench-gated MIS device of Claim 17 wherein a second aperture in the nonconductive layer overlies the second widened portion, the second aperture being filled with a gate metal such that the gate metal contacts gate material at a level no higher than the surface of the semiconductor chip.

19. The trench-gated MIS device of Claim 18 wherein the first and second widened portions are offset with respect to each other in a direction parallel to the first and second gate fingers.

20. A process of fabricating an MIS device comprising:

forming a trench in a surface of a semiconductor chip;

forming a nonconductive layer on a wall of the trench;

depositing a layer of a conductive gate material such that the gate material overflows onto the surface of the semiconductor chip outside the trench; and

etching the gate material such that a top surface of the gate material is reduced to a level below the surface of the semiconductor chip in all areas of the chip.

21. The process of Claim 20 wherein the etching is performed without a mask.

22. A process of fabricating an MIS device, the device comprising an active region and a termination region, comprising:

forming a trench mask over the surface of a semiconductor substrate, the substrate being doped with material of a first conductivity

type, the trench mask having an aperture defining the location of a termination trench to be formed;

etching through the aperture in the trench mask to form a termination trench in the substrate;

removing the trench mask;

forming a first nonconductive layer on a wall of the termination trench;

depositing a layer of a conductive gate material into the termination trench, the conductive gate material overflowing the surface of the substrate outside the termination trench;

etching the gate material without a mask such that a top surface of the gate material in the termination trench is reduced to a level below the surface of the substrate;

depositing a second nonconductive layer over the surface of the substrate,

forming a contact mask over the second nonconductive layer, the contact mask having a gate contact aperture;

etching the second nonconductive layer through the gate contact aperture in the contact mask to form a gate contact aperture in the second nonconductive layer;

removing the contact mask; and

depositing a second conductive layer over the second nonconductive layer, the second conductive layer extending through the gate contact aperture to make contact with the conductive gate material in the termination trench.

23. The process of Claim 22 wherein the contact mask has a substrate contact aperture, the process comprising etching the second nonconductive layer through the substrate contact aperture in the contact mask to form a substrate contact aperture in the second nonconductive layer, and wherein depositing a second conductive layer over the second nonconductive layer causes the second

conductive layer to extend through the substrate contact aperture to make contact with the substrate.

24. The process of Claim 23 comprising forming a metal mask over the second conductive layer, the metal mask having an aperture, and etching the second conductive layer through the aperture in the metal mask to form a first portion of the second conductive layer that is in electrical contact with the gate material and a second portion of the second conductive layer that is in electrical contact with the substrate, the first and second portions of the second conductive layer being electrically isolated from each other.

25. The process of Claim 22 wherein the process does not include a mask for etching a portion of an oxide layer to form a field oxide region in the termination region.

26. The process of Claim 22 comprising forming a body mask over the surface of the substrate, the body mask having an aperture, and implanting dopant of a second conductivity type into the substrate through the aperture in the body mask to form a body region.

27. The process of Claim 22 wherein the trench mask contains a second aperture in the active region and a third aperture in a channel stopper region, and wherein the process comprises etching the substrate through the second and third apertures to form an active trench in the active region and a channel stopper trench in the channel stopper region.

28. The process of Claim 27 comprising forming a source mask over the substrate, the source mask having an aperture over an area of the substrate adjacent to the active trench, and implanting dopant of the first conductivity type through the aperture in the source mask to form a source region of the MIS device.

29. The process of Claim 28 wherein the source mask comprises a second aperture in the channel stopper region and the process comprises implanting dopant of the first conductivity type into an area adjacent to the channel stopper trench.

30. The process of Claim 23 comprising implanting dopant of the second conductivity type through the substrate contact aperture in the second nonconductive layer to form a heavily-doped contact region in the substrate.

31. The process of Claim 27 wherein

depositing a layer of conductive gate material comprises depositing the conductive gate material into the channel stopper trench;

etching the gate material without a mask comprises reducing the surface of the gate material in the channel stopper trench to a level below the surface of the substrate;

the contact mask has a second aperture over the channel stopper trench;

the process comprises etching the second nonconductive layer through the second aperture in the contact mask to expose the surface of the conductive gate material in the channel stopper trench; and

depositing the second conductive layer comprises causing the second conductive layer to flow into the second aperture in the contact mask and to make electrical contact with the conductive gate material in the channel stopper trench.

32. The process of Claim 22 wherein

the second conductive layer comprises metal;

the trench mask comprises a second aperture;

the process comprises etching the substrate through the second aperture in the trench mask to form a Schottky diode trench in the substrate;

depositing a layer of a conductive gate material comprises depositing the conductive gate material into the Schottky trench;

the body mask covers the Schottky trench and an adjacent area of the substrate;

the contact mask has a second aperture over an area of the substrate adjacent to the Schottky trench;

the process comprises etching the second nonconductive layer through the second aperture in the contact mask to expose the area of the substrate adjacent to the Schottky trench; and

depositing the second conductive layer comprises causing the second conductive layer to fill the second aperture in the contact mask and to make electrical contact with the area of the substrate adjacent to the Schottky trench, thereby forming a Schottky diode.

33. The process of Claim 22 wherein the trench mask contains a second aperture in the active region, and wherein the process comprises etching the substrate through the second aperture to form an active trench in the active region.

34. The process of Claim 33 comprising:

depositing a polysilicon layer over the substrate;

introducing a dopant of a second conductivity type into the polysilicon layer;

forming a polysilicon mask over the polysilicon layer, the polysilicon mask defining the location of a polysilicon diode to be formed;

etching an area of the polysilicon layer not covered by the polysilicon mask;

removing the polysilicon mask;

forming a source mask, the source mask having a first aperture over an area of the substrate adjacent to the trench and a second aperture over a region of the polysilicon layer; and

implanting dopant of the first conductivity type through the first and second apertures in the source mask to form a source region of the MIS device and a terminal of a polysilicon diode.

35. The process of Claim 34 wherein:

depositing a second nonconductive layer is performed after implanting dopant of the first conductivity type through the first and second apertures in the source mask;

the contact mask has an anode aperture overlying an anode of the polysilicon diode and a cathode aperture overlying a cathode of the polysilicon diode;

the process comprises etching the second nonconductive layer through the anode and cathode apertures in the contact mask to form anode and cathode contact apertures in the second nonconductive layer, respectively; and

depositing a second conductive layer comprises causing the second conductive layer to flow into the anode and cathode contact apertures so as to make electrical contact with the anode and cathode, respectively, of the polysilicon diode.

36. The process of Claim 34 wherein

the polysilicon mask defines the location of a polysilicon MOSFET to be formed;

the trench mask contains a third aperture in the active region, the process comprising etching the substrate through the third aperture to form a polysilicon MOSFET trench; and

wherein the source mask has at least one opening defining a region within the polysilicon MOSFET.

37. The process of Claim 22 comprising:

forming a second contact mask over the second nonconductive layer, the second contact mask having a substrate contact aperture;

etching the second nonconductive layer through the substrate contact aperture in the second contact mask to form a substrate contact aperture in the second nonconductive layer; and

wherein depositing a second conductive layer over the second nonconductive layer causes the second conductive layer to extend through the substrate contact aperture to make contact with the substrate.

38. A process of fabricating an MIS device comprising:

providing a semiconductor substrate doped with dopant of a first conductivity type;

growing an epitaxial layer of a second conductivity type on a semiconductor substrate;

forming a trench mask over the surface of the epitaxial layer, the trench mask having a first aperture in an active region of the device and a second aperture in a termination region of the device, the termination region being located between the active region and a channel stopper region;

etching the epitaxial layer through the first and second apertures in the trench mask to form first and second trenches, the second trench being substantially wider than the first trench;

removing the trench mask;

forming a first nonconductive layer on a wall of the first and second trenches;

depositing a layer of a conductive gate material into the first and second trenches, the layer of conductive gate material overflowing the surface of the substrate outside the trenches;

etching the conductive gate material such that a top surface of the conductive gate material in the first trench is reduced to a level below the surface of the substrate and the conductive gate material in the second trench is substantially removed;

depositing a second nonconductive layer over the surface of the epitaxial layer and over the gate material in the first trench and into the second trench;

forming a contact mask over the second nonconductive layer, the contact mask having a substrate contact aperture and a gate contact aperture;

etching the second nonconductive layer through the apertures in the contact mask to form a substrate contact aperture and a gate contact aperture in the second nonconductive layer;

removing the contact mask; and

depositing a second conductive layer over the second nonconductive layer, the second conductive layer extending through the substrate contact aperture to make contact with the substrate and through the gate contact aperture to make contact with the conductive gate material.

39. The process of Claim 38 comprising:

forming a metal mask over the second conductive layer, the metal mask having an aperture; and

etching the second conductive layer through the aperture in the metal mask.

40. A trench-gated MIS device comprising:

a semiconductor substrate generally doped with a dopant of a first conductivity type, a trench being formed in an active region of the substrate;

an insulating layer disposed along a wall of the trench, the trench containing a conductive gate material, a surface of the gate material being at a level below a surface of the substrate;

a nonconductive layer overlying the surface of the substrate;

a conductive layer overlying the nonconductive layer, the conductive layer comprising a current-carrying portion and a gate bus portion, the current-carrying portion and the gate bus portion being electrically isolated from each other, the nonconductive layer having an aperture through which the current-carrying portion of the metal layer is in electrical contact with the substrate in the active region of the device,

wherein the thickness of the nonconductive layer underlying the gate bus portion of the conductive layer is substantially the same as the thickness of the nonconductive layer underlying the current-carrying portion of the conductive layer.

41. The trench-gated MIS device of Claim 40 further comprising a second trench in the substrate, the second trench being located beneath the gate bus portion and containing conductive gate material, a surface of the gate material in the second trench being at a level below the surface of the substrate, the nonconductive layer having a second aperture through which the gate bus portion of the conductive layer is in electrical contact with the gate material in the second trench.

42. The trench-gated MIS device of Claim 40 wherein the conductive layer comprises metal, the device further comprising a second trench in the substrate, the insulating layer being disposed along a wall of the trench, the second trench containing conductive gate material, the nonconductive layer having a second aperture overlying the second trench and an adjacent area of the substrate, the current-carrying portion of the conductive layer forming a Schottky interface with the substrate at the area of the substrate adjacent to the second trench.

43. The trench-gated MIS device of Claim 42 further comprising a third trench in the substrate, the third trench being located beneath the gate bus portion and containing conductive gate material, a surface of the gate material in the third trench being at a level below the surface of the substrate, the nonconductive layer having a third aperture through which the gate bus portion of the conductive layer is in electrical contact with the gate material in the third trench.

44. A trench-gated MIS device comprising an active device region and a channel stopper region, the device comprising:

a semiconductor substrate generally doped to a conductivity of first type;

an epitaxial layer overlying the substrate;

a first trench formed in the epitaxial layer in the active region of the device, an insulating layer being disposed along a wall of the trench, the trench containing a conductive gate material, a surface of the conductive gate material being at a level below a surface of the epitaxial layer;

a second trench formed in the epitaxial layer at a location between the active region and the channel stopper region, the second trench being substantially wider than the first trench in at least one location of the second trench;

a nonconductive layer overlying the epitaxial layer in the active region, the nonconductive layer having an aperture in the active region;

a conductive layer overlying the nonconductive layer, the conductive layer comprising a current-carrying portion and a gate bus portion, the current carrying portion being located in the active region, the gate bus portion being located between the active region and the channel stopper region, the current-carrying portion extending through the aperture in the nonconductive layer to make electrical contact with the epitaxial layer,

wherein the thickness of the nonconductive layer underlying the gate bus portion of the conductive layer is substantially the same as the thickness of the nonconductive layer underlying the current-carrying portion of the conductive layer.

45. The trench-gated MIS device of Claim 44 further comprising a third trench in the epitaxial layer located beneath the gate bus portion, the third trench containing conductive gate material, the nonconductive layer having a second aperture through which the gate bus portion of the conductive layer is in electrical contact with the conductive gate material in the third trench.

46. A trench-gated MIS device having an active area and a gate bus area, the device comprising:

a semiconductor substrate, a first trench being formed in the substrate in the active area and a second trench being formed in the substrate in the gate bus region, an insulating layer being disposed along a wall of each of the first and second trenches, each of the first and second trenches containing a conductive gate material, the second trench being wider and deeper than the first trench in at least one location of the second trench, the conductive gate material in the second trench being in electrical contact with a gate bus;

at least one pair of protective trenches formed on opposite sides of the second trench, the second trench being deeper than the protective trenches, each of the protective trenches containing conductive gate material, the conductive gate material in the protective trenches being electrically connected to the conductive gate material in the second trench.

47. The trench-gated MIS device of Claim 46 wherein a mesa between at least one of the protective trenches and the second trench is allowed to electrically float.

48. The trench-gated MIS device of Claim 46 wherein the protective trenches have substantially the same width and depth as the first trench.